SEMICONDUCTOR MEMORY DEVICES HAVING OFFSET TRANSISTORS AND METHODS OF FABRICATING THE SAME

Abstract of the Disclosure

Semiconductor memory devices are provided that comprise unit memory cells. The unit memory cells include a first planar transistor in a semiconductor substrate, a vertical transistor disposed on the first planar transistor and a second planar transistor in series with the first planar transistor. The first planar transistor and the second planar transistor may have different threshold voltages. The semiconductor memory device may further include word lines. One of these word lines may form the gate of the second planar transistor a unit memory cell.

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